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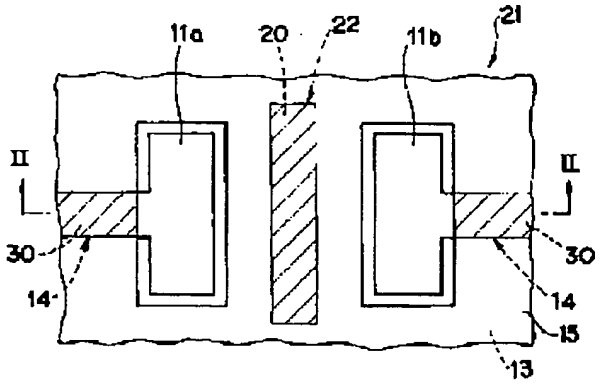
(54) [Title of the Invention] Printed Circuit Board and Manufacturing Method Thereof

(57) [Summary]

[Composition of the Invention] A printed circuit board 21 has an identification mark pattern used for inspection of state of mounted components that is formed simultaneously with formation of a circuit pattern 14. At least the surface side of this mark pattern is subjected to oxidation treatment to form the identification mark by forming a discolored oxide film 20.

[Result of the Invention] It is possible to form the identification mark with extremely high accuracy. Therefore it is possible to easily and accurately inspect the mounting state of components carried at high density, and also it becomes possible to inspect mounting accuracy with respect to small size components. Moreover, identification mark pattern formation and circuit pattern formation are carried out during the same step, and it is possible to manufacture the printed circuit board extremely inexpensively.



[Scope of the Patent Claims]
[Claim 1] A printed circuit board comprising an electrically conductive layer of a certain circuit pattern on a substrate and an identification mark formed between lands for testing of mounting state of an electronic component carried on the lands,

wherein the identification mark is formed by discoloration treatment at least of the surface side of the conductive layer formed of a certain pattern, and the identification mark is formed simultaneously with formation of the conductive layer.

[Claim 2] A printed circuit board comprising an electrically conductive layer of a certain circuit pattern on a substrate and an identification mark formed between lands for testing of mounting state of an electronic component carried on the lands, the electronic component being connected to the lands used for carrying the electronic components;

wherein the identification mark is formed by discoloration treatment at least of the surface side of the conductive layer formed of a certain pattern, and the identification mark is formed simultaneously with formation of the conductive layer.

[Claim 3] A method for manufacture of a printed circuit board comprising:

a step of forming a first electrically conductive layer into a certain circuit pattern on a substrate, and simultaneously forming a certain second electrically conductive layer between planned regions of formation of lands used for carrying electronic compounds of a first electrically conductive layer; and

a step thereafter of discoloration treatment, and thereafter of leaving behind a discolored film at least at the surface side of the second electronically conductive layer as an identification mark used for testing of mounting state of the electronic components.

[Detailed Description of the Invention]
[0001]
[Industrial Field of Use] The present invention relates to a printed circuit board and a method for manufacture of such, and the present invention particularly relates to a printed circuit board and a method for manufacture of this printed circuit board that has a mark for identification of the mounting state of the electronic components after mounting.

[0002]
[Earlier Technology] Generally an identification mark called a "silk [*screen printing mark*]" is provided on a printed circuit board in order to inscribe on a substrate the type of electronic components (i.e. semiconductor IC chips and the like), to indicate attachment locations, to show reference numbers for each component, to indicate the soldering method, to act as an ID mark, to check the mounting state of components, to prevent solder bridging, and the like.

[0003] The major conventional method for forming this type of identification mark has been printing either using UV curing or thermal curing. However, due to higher density of surface mounting and smaller size of chip components, the need has arisen recently for highly accurate formation of the identification mark in order to check mounting state of components. Formation of the identification mark by the printing method results in extremely poor accuracy, ±150 to ±200 μm, and the printing method has become unsuitable for the above mentioned application. This is explained below in detail.

[0004] For example, as shown in Figure 14 through Figure 16, an identification mark (silk [*screen printing mark*]) 12 for inspection use is carried between a chip component carrying land 11a and a chip component carrying land 11b on a printed circuit board 1 below a chip component 10. Mounting positional accuracy is inspected based on displacement of the chip component 10 relative to this mark 12. Furthermore, the mark 12 is formed on a solder resist layer 15 applied to a region outside of the lands 11a and 11b.

[0005] In this case, as shown in Figure 16, a wiring pattern 14 is formed by patterning a conductor layer on an insulation substrate 13. Thereafter the solder resist 15 is formed at the parts other than the lands 11a and 11b formed on either tip part of the wiring pattern 14.

[0006] Thereafter the mark 12 is formed (e.g. by screen printing and the like) on the solder resist 15 in the vicinity of the above mentioned lands 11a and 11b (to be precise, between the lands 11a and 11b carrying the chip component 10).

[0007] During the inspection, position of the chip component 10 after mounting and position of the mark 12 are recognized visually or are recognized by image processing using a CCD camera. Mounting accuracy of the chip component 10 is inspected based on the relative positional relationship of the chip component 10 and the mark 12.

[0008] However, since the identification mark 12 is formed on the solder resist 15 of the conventional printed circuit board, positional accuracy of the mark 12 is poor, and in recent years there have been instances when the conventional method can not be used for circuit boards of increasingly high density. That is to say, this problem occurs because the accuracy of printing during formation of the mark 12 is not sufficient with respect to the lands 11a and 11b.

[0009] That is to say, the printing accuracy for screen printing is ±150 to ±200 μm, and when for example an extremely small chip is mounted for which the spacing between the lands 11a and 11b is about 150 μm, as shown in Figure 17, problems occur, for example, such as formation of the mark toward the side of the chip component 10 so that the inspection for mounting accuracy can not be carried out correctly.

[0010] Therefore the identification mark 12 is presently printed upon the solder resist 15; this printing step is troublesome for the above mentioned reasons; and high accuracy is required. However, since the accuracy of printing is poor, as long as the mark 12 is used, most inspection processes result in failure even if the mounting accuracy of the chip component 10 is increased. It is thus not possible to plan for an increase of density of the printed circuit board.

[0011]
[Object of the Invention] The object of the present invention is to provide a printed circuit board and a manufacturing method for this printed circuit board capable of ready inspection of components mounted at high density while making possible simple and inexpensive formation of an identification mark with high accuracy.

[0012]
[Composition of the Invention] That is to say, the present invention is a printed circuit board comprising an electrically conductive layer of a certain circuit pattern on a substrate and an identification mark formed between lands for testing of mounting state of an electronic component carried on the lands, wherein the identification mark is formed by discoloration treatment at least of the surface side of the conductive layer formed of a certain pattern, and the identification mark is formed simultaneously with formation of the conductive layer.

[0013] Moreover, the present invention provides a printed circuit board comprising an electrically conductive layer of a certain circuit pattern on a substrate and an identification mark formed between lands for testing of mounting state of an electronic component carried on the lands, the electronic component being connected to the lands used for carrying the electronic components; wherein the identification mark is formed by discoloration treatment at least of the surface side of the conductive layer formed of a certain pattern, and the identification mark is formed simultaneously with formation of the conductive layer.

[0014] Furthermore, the present invention provides a method for manufacture of a printed circuit board comprising: a step of forming a first electrically conductive layer into a certain circuit pattern on a substrate, and simultaneously forming a certain second electrically conductive layer between planned regions of formation of lands used for carrying electronic compounds of a first electrically conductive layer; and a step thereafter of discoloration treatment, and thereafter of leaving behind a discolored film at least at the surface side of

the second electronically conductive layer as an identification mark used for testing of mounting state of the electronic components.

[0015]
[Working Examples] Working examples of the present invention are explained below.

[0016] Figure 1 through Figure 12 show a working example of the present invention. A printed circuit board 21 of the present working example is formed somewhat in the same manner as that of the conventional technology in that a wiring pattern 14 is formed by patterning a conductive layer (e.g. copper layer) on an insulation substrate 13. However, the working example of the present invention fundamentally differs from the conventional technology in that, as shown in Figure 1 through Figure 3, an identification mark 22 (formed from the conductive layer 23 simultaneously with formation of the wiring pattern 14) is provided between chip component mounting lands 11a - 11b formed at either tip part of the wiring pattern 14; and this [*identification mark 22*] is subjected to discoloration treatment (e.g. to a color combining red and black) to form an oxide film 20 of the surface of this [*identification mark 22*].

[0017] Moreover, when the above mentioned oxide film 20 is formed by a below mentioned chemical treatment, an oxide film 30 is also formed at the same time on the surface of the wiring pattern 14. This oxide film 30 is selectively removed at the region of the lands 11a and 11b by etching treatment while using masking by a solder resist 15 formed to cover areas other than the lands 11a and 11b, thereby exposing the conductive layer.

[0018] Furthermore, the above mentioned mark 22 is formed independently of the wiring pattern 14, and the oxide film (insulation film) 20 is present on the surface thereof. Thus there is no need for providing the solder resist 15 upon the mark 22.

[0019] The identification mark 22, in the above mentioned manner and according to the present invention, is formed by the oxide film (e.g. formed from a combination of red Cu_2O and black CuO) 20 on the surface, for example, of a copper layer 23 of a certain pattern during the same step of formation as the wiring pattern (e.g. copper pattern) 14, and identification is quite possible through the resist 15 on the printed circuit board 21. Although detection errors readily occur if there is dirt on the copper layer 23, since an oxide film 20 is formed on the copper layer 23, the effect of dirt is eliminated by color [*of the oxide film 20*], and reliable detection becomes possible.

[0020] Thus as shown in Figure 4 and Figure 5, regions A and B are imaged by a CCD camera 50, and while the areas of the regions are monitored, the component 10 and the mark 22 are distinguished from one another on the image. By this means, clear distinction is possible due to sufficient contrast between color of the component and color of the mark 22 at the regions A and B in the monitored image.

[0021] In this manner, post-mounting position of the chip component 10 and position of the mark 22 are recognized by image processing (or visually), and mounting precision of the chip component 10 is inspected based on relative positions of the chip component 10 and the inspection mark 22.

[0022] The mark 22 of the pattern (i.e. conductive layer 23) according to the present working example is formed simultaneously with formation of the above mentioned wiring pattern 14 from the same conductive layer as that of the wiring pattern 14 (i.e. during the same step as that of formation of lands 11a and 11b). Thus it is possible to form [*mark 22*] with an accuracy (e.g. ±10 μm) much higher than that of the conventional mark formed by screen printing. It is thus possible to accurately and readily inspect mounting state of the chip component 10 mounted at high density, and it becomes also possible to inspect mounting precision for a small size chip.

[0023] Moreover, since the mark 22 is formed simultaneously with formation of the wiring pattern 14, it is possible to manufacture the printed circuit board very inexpensively.

[0024] The manufacturing process of the printed circuit board of the present working example will be explained next using Figure 6 through Figure 11.

[0025] Firstly, as shown in Figure 6 and Figure 9, the electrically conductive layer (e.g. a copper layer of about 40 μm thickness) is formed as a circuit pattern on the substrate 13. Simultaneous with this layer formation, a conductive layer (e.g. a copper layer of about 40 μm thickness) 23 is formed of a certain pattern between the opposing lands 11a and 11b used for component mounting.

[0026] Thereafter the surface of the substrate is subjected to bush rubbing (buffing), oxidation treatment, and surfacing processing.

[0027] After water washing-rinsing with purified water, the electrically conductive layers 14 and 23 are subjected to chemical oxidation treatment. As shown in Figure 7 and Figure 10, the oxide films 30 and 20 (e.g. copper oxide films as combinations of Cu_2O and CuO of several μm thickness) are formed respectively on the surfaces. Part of the oxide film 20 becomes discolored at this time to form the identification mark 22.

[0028] The oxidation treatment is carried out under the below described conditions.
Composition of the oxidation agent liquid: 40 g/L sodium hydroxide and 16 g/L potassium persulfate in 1 L of purified water
Treatment conditions: 0.5 - 2.0 minutes immersion time at a liquid temperature of 60 ± 5°C.

[0029] This oxidation treatment is followed by rinsing with purified water and then drying for 5 minutes at 80°C.

[0030] Thereafter a photosensitive solder resist applied by screen printing, roll coating, curtain coating, electrostatic coating, and the like is used to coat the substrate 13. During this step, printing can be readily carried out, in the case of screen printing, by use of a screen of 100 - 150 mesh size, or by solid printing.

[0031] Thereafter the solid printed solder resist is dried (semi-cured) for 20 to 30 minutes at 80°C to 90°C to form a resist of 10 - 20 μm layer thickness. Thereafter an exposure mask is used to expose a certain pattern of the solder resist at an energy [*density*] of 300 - 600 mJ/cm^2 using a high pressure mercury lamp (5 - 7 kW).

[0032] Thereafter development is carried out for 10 - 30 seconds in 1 - 3% Na_2CO_3 aqueous solution (temperature = 40°C to 50°C) to remove the unnecessary parts. Then a further 30 - 40 minute post cure at 150°C is carried out to leave behind a certain pattern of the solder resist 15 except at the lands 11a and 11b as shown in Figure 8 and Figure 11.

[0033] Thereafter if there is a need for a silk [*screen printing mark*] that has a function other than providing for detection of component mounting state, this can be formed by the normal method on the above mentioned solder resist.

[0034] Thereafter [*the circuit board*] in the state shown in Figure 8 and Figure 11 undergoes surface treatment by an acid such as hydrochloric acid, sulfuric acid, and the like, thereby removing the non-solder resist areas (i.e. the regions of the lands 11a and 11b) and etching using the solder resist as a mask. The oxide film 30 is partially removed to expose the conductive layer of the lands 11a and 11b as shown in Figure 1 and Figure 2. Furthermore, since this surface treatment itself is normally carried out as surfacing processing, the manufacturing process is not changed.

[0035] A certain chip component 10 is surface mounted on the printed circuit board 21 manufactured in this manner as shown in Figure 4 and Figure 5. At this time, preparatory solder or cream solder (not illustrated) is printed on the lands 11a and 11b, then the component 10 is placed, the [*printed circuit board 21*] is loaded in a reflow furnace, and the component 10 is connected (mounted) by solder reflow.

[0036] As made clear by the above mentioned manufacturing process, the conductive layer 23 that becomes the mark 22 is formed simultaneously with formation of the wiring pattern 14 from the same conductive layer during the step of Figure 6 and Figure 9. Thus formation is possible with an extremely high accuracy (e.g. ± 10 μm) in comparison to the conventional mark formed by screen printing. Moreover, pattern formation of the mark 22 and formation of the wiring pattern 14 are carried out during the same step, and extremely inexpensive manufacture of the printed circuit board is possible.

[0037] It is possible to form the mark 22 just by oxidation treatment of the conductive layer 23 (e.g. providing a mixed color of red and black), and this color has sufficient contrast relative to that of the component 10.

[0038] Furthermore, the oxide layer 30 on the wiring pattern is discolored simultaneously as described previously. Thus recognition becomes readily carried out from the exterior through the resist 15, and this is advantageous for repair and inspection by pattern inspection.

[0039] Furthermore, the printed circuit board 21 of the present working example can be used for a multi-layer printed circuit board.

[0040] During the above mentioned working example, the mark 22 was formed independently of the wiring pattern 14 between the lands 11a and 11b. However it is also possible, for a normal wiring pattern 22A between the lands 11a and 11b, as shown in Figure 12, to use a partial widening 22B of the wiring pattern 22A between the lands 11a and 11b as the identification mark 22.

[0041] Moreover, as shown in Figure 13, within the wiring pattern 22A running between the lands 11a and 11b, two wide diameter (e.g. the circular parts 22B) parts may be formed from the wiring pattern 22A to the exterior of width D of the lands 11a and 11b; and these parts may be used are identification marks 22.

[0042] The examples of Figure 12 and Figure 13, in the same manner as the working example shown in Figure 1 and due to formation of the wiring pattern 22A between the lands 11a and 11b, make possible accurate inspection of mounting accuracy of the chip component 10 mounted at high density, make possible manufacture of an extremely inexpensive printed circuit board, and also make possible formation of a high density wiring pattern.

[0043] Although working examples of the present invention were explained above, further changes of the above mentioned working examples are possible based upon the technical concepts of the present invention.

[0044] For example, various types of changes are permissible for the pattern, material, and the like of the above mentioned identification pattern 22, and it is also possible to change the composition thereof (and thus the color thereof) or the oxidation treatment liquid used for the oxide film 20 of the conductive surface.

[0045] Moreover, it is possible to provide the oxide film 20 only at the identification mark and not to provide the [*oxide film of the*] circuit pattern, for example, by shielding the circuit pattern with a mask material during the oxidation treatment. Although it is then permissible to oxidize the entire layer of the identification mark, normally an electrically conductive layer is left behind in the same manner as the above mentioned examples.

[0046] Moreover, it is possible to cause discoloration of the electrically conductive layer by treatments without restriction to just this oxide film 20. The above mentioned mark, that is not the above mentioned identification mark, that has the discolored film formed in this manner, can comprise a number or another mark indicating the type, etc. of the component.

[0047] The solder resist 15, in the case of the above mentioned screen printing, can be any type such as the UV curing type or heat curing type. In the case of the photographic method, this may be the UV curing type. It is possible to change the etching method or the etching liquid for the oxide film at the lands 11a and 11b using masking by the solder resist.

[0048] In addition, use of various types of materials or shapes of the constituent parts of the above mentioned printed circuit board, various types of mounting components, and the like is permissible.

[0049]
[Result of the Use of the Invention] As explained previously, identification mark pattern formation and circuit pattern formation are carried out simultaneously, and at least the surface side of this mark pattern is subjected to discoloration treatment to form the identification mark pattern. It is possible to form [*the identification mark*] with extremely high accuracy in comparison to the conventional mark formed by screen printing. It is thus possible to readily and accurately inspect mounting state of components mounted at high density and also inspect mounting accuracy of small size components.

[0050] Moreover, formation of the pattern of the identification mark and formation of circuit pattern are carried out during the same step, and it is possible to manufacture the printed circuit board extremely inexpensively.

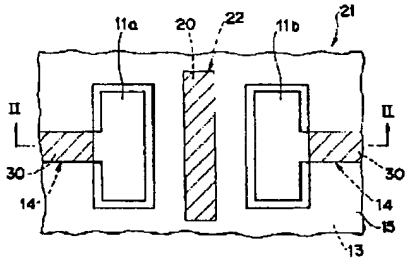
[Simple Description of the Figures]
[Figure 1] This is a top planar view of relevant parts of the printed circuit board according to the working example of the present invention.
[Figure 2] This is a II - II cross-sectional drawing of Figure 1 of the same printed circuit board.
[Figure 3] This is a partial magnified view of Figure 2.
[Figure 4] This is a top planar view of relevant parts showing the inspection area during inspection of mounting state of the electronic component mounted on the same printed circuit board.
[Figure 5] This is a cross-sectional drawing corresponding to the V - V line of Figure 4 at the time of the same inspection.
[Figure 6] This is a top planar view of relevant parts showing conditions after formation of the electrically conductive circuit and the identification mark pattern during the manufacturing steps of the same printed circuit board.

[Figure 7] This is a top planar view of relevant parts showing conditions after discoloration of the copper layer by oxidation treatment of the electrically conductive circuit and the identification mark pattern during the manufacturing steps of the same printed circuit board.
[Figure 8] This is a top planar view of relevant parts showing conditions after formation of the solder resist during the manufacturing steps of the same printed circuit board.
[Figure 9] This is a cross-sectional drawing at IX - IX of Figure 6.
[Figure 10] This is a cross-sectional drawing at X - X of Figure 7.
[Figure 11] This is a cross-sectional drawing at XI - XI of Figure 8.
[Figure 12] This is a top planar view of relevant parts showing the printed circuit board according to another working example of the present invention.
[Figure 13] This is a top planar view of relevant parts showing the printed circuit board according to yet another working example of the present invention.
[Figure 14] This is a tilted-perspective view of relevant parts showing conditions of the mounted electronic component on the conventional printed circuit board.
[Figure 15] This is a top planar view of relevant parts of the same printed circuit board.
[Figure 16] This is a cross-sectional drawing at XVI - XVI of Figure 15 of the same printed circuit board.
[Figure 17] This is a top planar view of relevant parts showing positional displacement condition of the silk [*screen printing mark*] (identification mark) on the same printed circuit board.

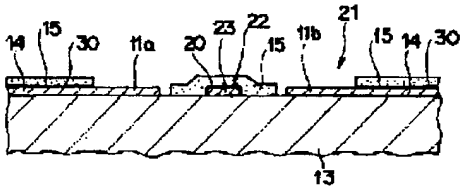
[Explanation of Number Coding]

1, 21	...	printed circuit board
10	...	electronic (chip) component
11a , 11b	...	land used for mounting the component
12, 22	...	identification mark (silk [*screen printing mark*])
14	...	wiring pattern
15	...	solder resist
20, 30	...	oxide film (discolored film)
23	...	conductive layer (electrically conductive layer)
30	...	CCD camera

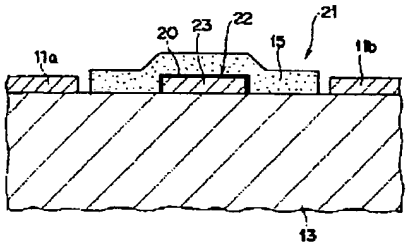
[Figure 1]



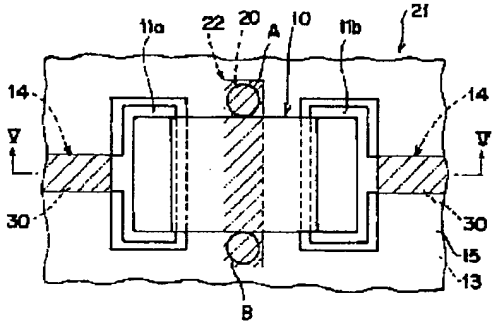
[Figure 2]



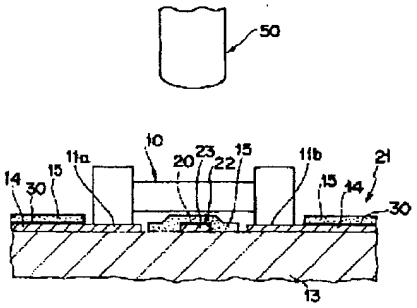
[Figure 3]



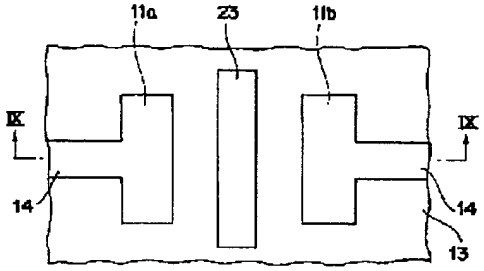
[Figure 4]



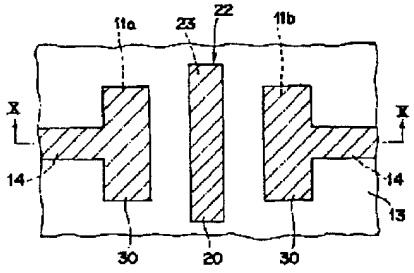
[Figure 5]



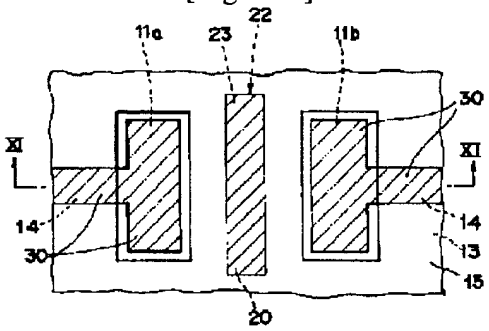
[Figure 6]



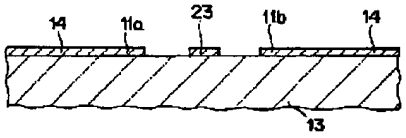
[Figure 7]



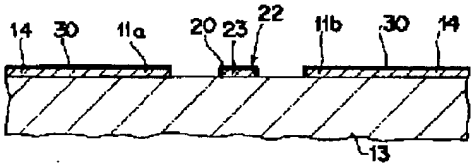
[Figure 8]



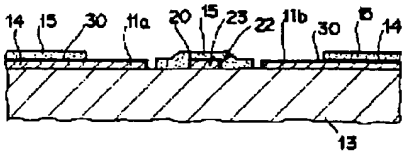
[Figure 9]



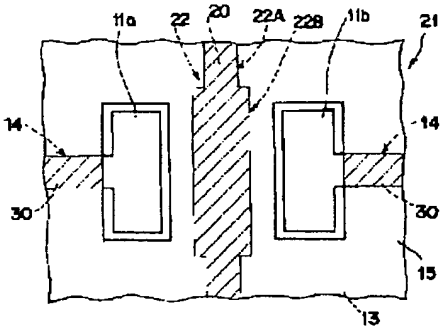
[Figure 10]



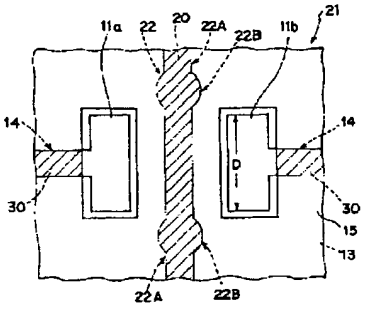
[Figure 11]



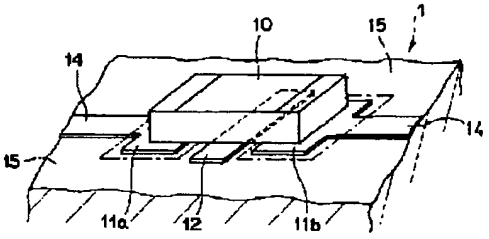
[Figure 12]



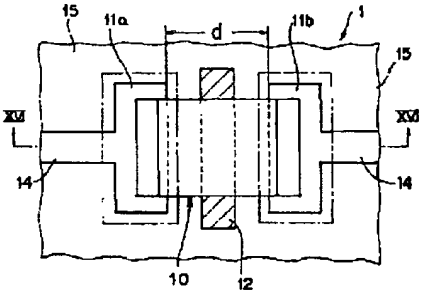
[Figure 13]



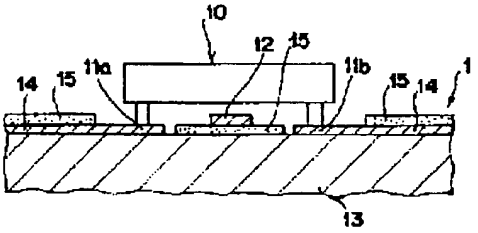
[Figure 14]



[Figure 15]



[Figure 16]



[Figure 17]